WHAT IS CLAIMED IS:

1. A chemical-mechanical polishing process, comprising the steps of:

forming a first metal line layer and a dielectric layer over a semiconductor substrate;

polishing the dielectric layer to form a planar surface; and

forming a thin cap layer over the dielectric layer.

2. The process of claim 1, wherein the step of forming the first metal line layer includes depositing doped polysilicon.

3. The process of claim 1, wherein the step of forming the dielectric layer includes a high-density plasma chemical vapor deposition (HDPCVD) method.

4. The process of claim 1, wherein the step of forming the dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

5. The process of claim 1, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

6. The process of claim 1, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

7. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silicane (SiH_4) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

8. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with

tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

9. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

10. The process of claim 1, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

11. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon dioxide.

12. The process of claim 1, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

13. The process of claim 1, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

14. A method of forming a metallic interconnect, the method comprising the steps of:

providing a semiconductor substrate having a first metallic line thereon;

forming a first dielectric layer over the substrate and the first metallic line;

forming a second dielectric layer over the first dielectric layer;

polishing the surface of the second dielectric layer;

forming a cap layer over the second dielectric layer;

forming a via opening through the first dielectric layer, the second dielectric layer and the cap layer, wherein the opening exposes the first metallic line; and

forming a second metallic line over the cap layer such that the second metallic line couples electrically with the first metallic line through the via.

15. The method of claim 14, wherein the step of forming the first metal line includes depositing doped polysilicon.

16. The method of claim 14, wherein the step of forming the first dielectric layer includes a high-density plasma chemical vapor deposition (HDPCVD) method.

17. The method of claim 14, wherein the step of forming the second dielectric layer includes a plasma-enhanced chemical vapor deposition (PECVD) method.

18. The method of claim 14, wherein the step of forming the first dielectric layer includes depositing silicon dioxide.

19. The method of claim 14, wherein the step of forming the second dielectric layer includes depositing silicon dioxide.

20. The method of claim 14, wherein the step of polishing the dielectric layer includes a chemical-mechanical polishing method.

21. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition (PECVD) method with silane (SiH_4) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

22. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition (CVD) method with

tetra-ethyl-ortho-silicate (TEOS) as main reactive agent such that the silicon oxide layer has a thickness of about 1000-3000Å, and can be adjusted according to design rules.

23. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicane (SiH_4) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

24. The method of claim 14, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition (CVD) method with silicon dichlorohydride (SiH_2Cl_2) as main reactive agent such that the silicon nitride layer has a thickness of about 100-3000Å, and can be adjusted according to design rules.

25. The method of claim 14, wherein the step of forming the cap layer includes depositing silicon dioxide.

26. The method of claim 14, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

27. The process of claim 14, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).